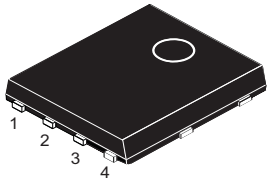
STL220N3LLH7

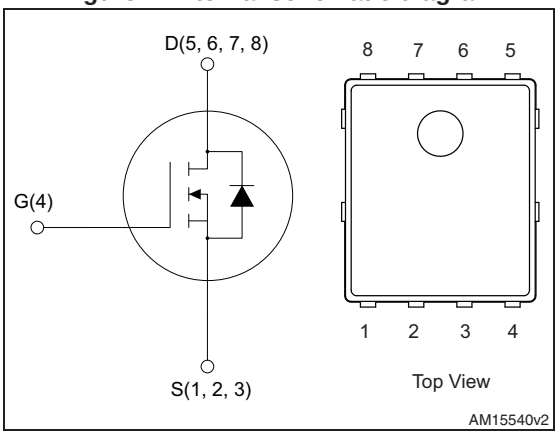
N-channel 30 V, 0.00081 Ω typ., 50 A STripFET™ VII DeepGATE™ Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data



PowerFLAT™5x6

Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max	I_D
STL220N3LLH7	30 V	0.0011 Ω	50 A

- Very low on-resistance
- Very low Q_g
- High avalanche ruggedness

Applications

- Switching applications

Description

This device exhibits low on-state resistance and capacitance for improved conduction and switching performance.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL220N3LLH7	220N3LL7	PowerFLAT™ 5x6	Tape and reel

This is information on a product in full production. www.st.com

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	± 20	V
I_D(1)	Drain current (continuous) at T_C = 25 °C	220	A
I_D(1)	Drain current (continuous) at T_C = 100 °C	160	A
I_{DM}(1)(2)	Drain current (pulsed)	880	A
I_D(3)	Drain current (continuous) at T_{pcb} = 25 °C	50	A
I_D(3)	Drain current (continuous) at T_{pcb} = 100 °C	32	A
I_{DM}(2)(3)	Drain current (pulsed)	200	A
P_{TOT}(1)	Total dissipation at T_C = 25 °C	113	W
P_{TOT}(3)	Total dissipation at T_{pcb} = 25 °C	4	W
T_j	Max. operating junction temperature	-55 to 150	°C

1. This value is rated according to R_{thj-c}
2. Pulse width limited by safe operating area.
3. This value is rated according to $R_{thj-pcb}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pcb}$(1)	Thermal resistance junction-pcb max	31.3	°C/W
$R_{thj-case}$	Thermal resistance junction-case max	1.1	°C/W

1. When mounted on FR-4 board of 1 inch², 2oz Cu, t < 10 sec

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 μA, V_{GS} = 0	30			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V V_{DS} = 24 V			1	μA
I_{GSS}	Gate-body leakage current	V_{GS} = ± 20 V, V_{DS} = 0			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 μA	1.2		2.2	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 25 A		0.00081	0.0011	Ω
		V_{GS} = 4.5 V, I_D = 25 A		0.00115	0.0015	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	8650	-	pF
C_{oss}	Output capacitance		-	2400	-	pF
C_{rss}	Reverse transfer capacitance		-	72	-	pF
Q_g	Total gate charge	V_{DD} = 15 V, I_D = 50 A, V_{GS} = 4.5 V (see *Figure 14*)	-	46	-	nC
Q_{gs}	Gate-source charge		-	26	-	nC
Q_{gd}	Gate-drain charge		-	10	-	nC
R_g	Intrinsic gate resistance	f=1 MHz	-	0.61	1.8	Ω

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 15 V, I_D = 25 A, R_G = 4.7 Ω, V_{GS} = 4.5 V	-	55	-	ns
t_r	Rise time		-	115	-	ns
$t_{d(off)}$	Turn-off delay time		-	70	-	ns
t_f	Fall time		-	51	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		50	A
I_{SDM} (1)	Source-drain current (pulsed)		-		200	A
V_{SD} (2)	Forward on voltage	I_{SD} = 50 A, V_{GS} = 0	-		1	V
t_{rr}	Reverse recovery time	I_D = 50 A, di/dt = 100 A/μs V_{DD} = 24 V	-	66		ns
Q_{rr}	Reverse recovery charge		-	101		nC
I_{RRM}	Reverse recovery current		-	3.1		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

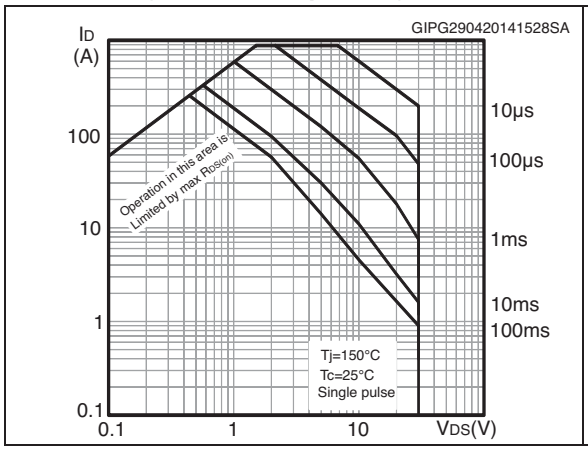


Figure 3. Thermal impedance

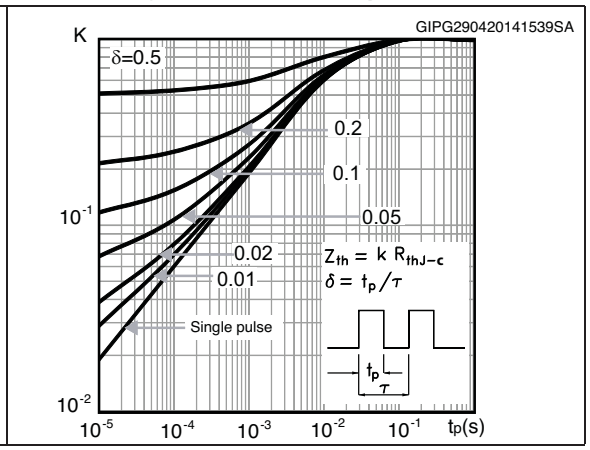


Figure 4. Output characteristics

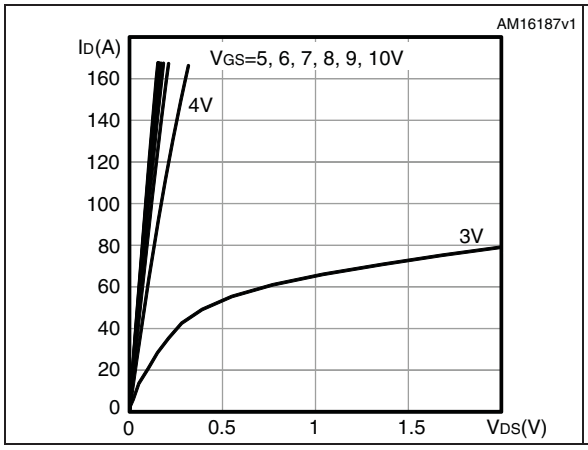


Figure 5. Transfer characteristics

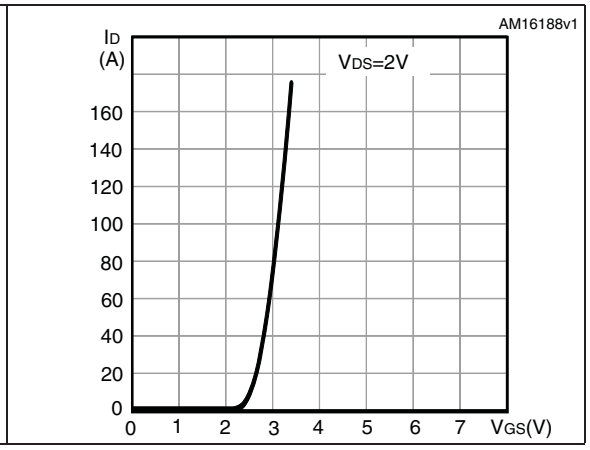


Figure 6. Gate charge vs gate-source voltage

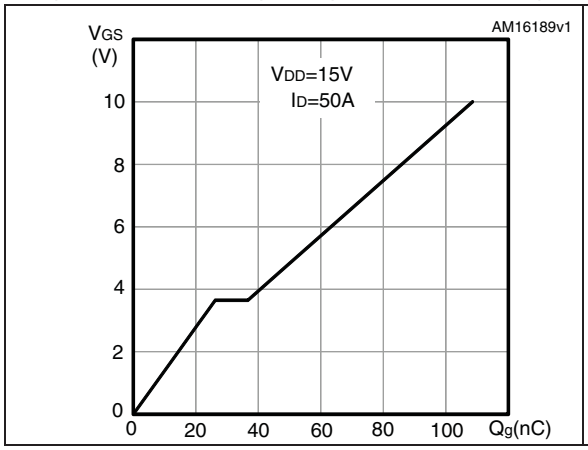


Figure 7. Static drain-source on-resistance

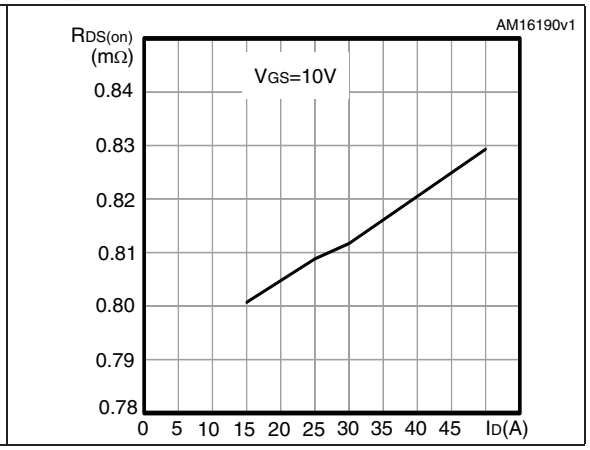


Figure 8. Capacitance variations

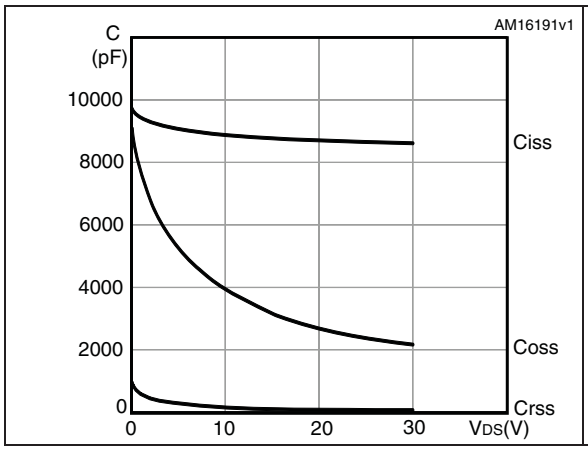


Figure 9. Normalized gate threshold voltage vs temperature

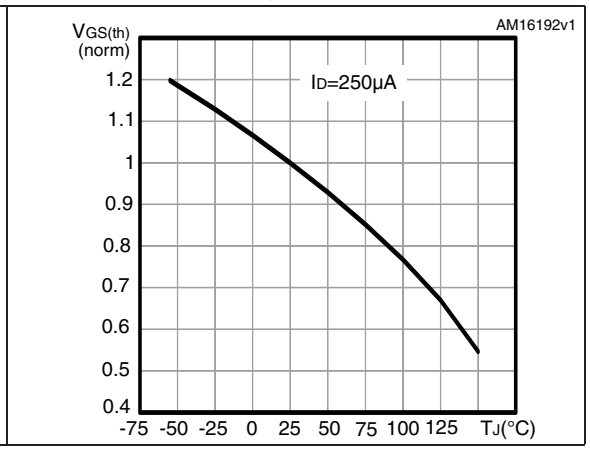


Figure 10. Normalized on-resistance vs temperature

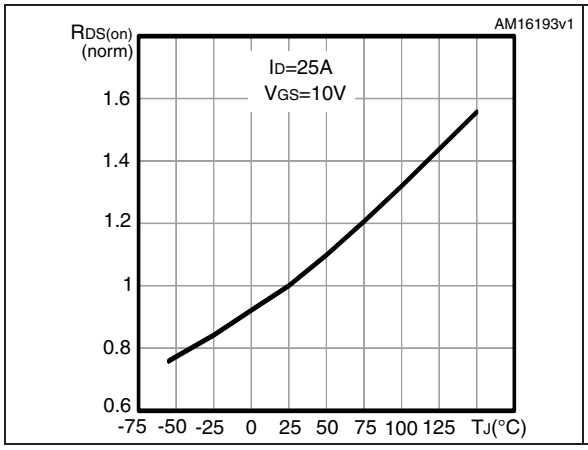


Figure 11. Normalized $V_{(BR)DSS}$ vs temperature

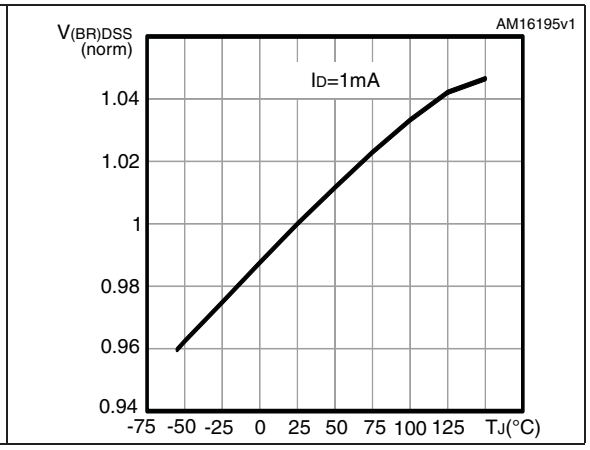
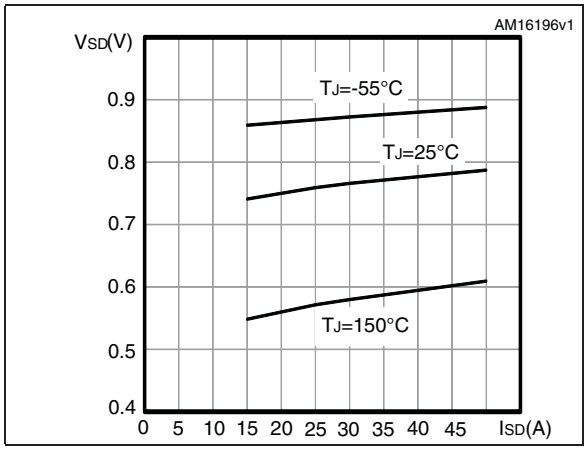


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

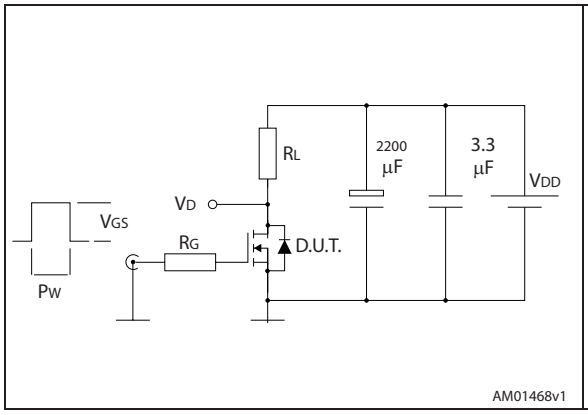


Figure 14. Gate charge test circuit

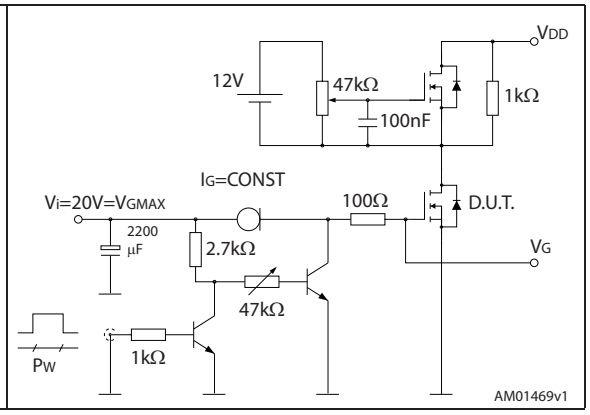


Figure 15. Test circuit for inductive load switching and diode recovery times

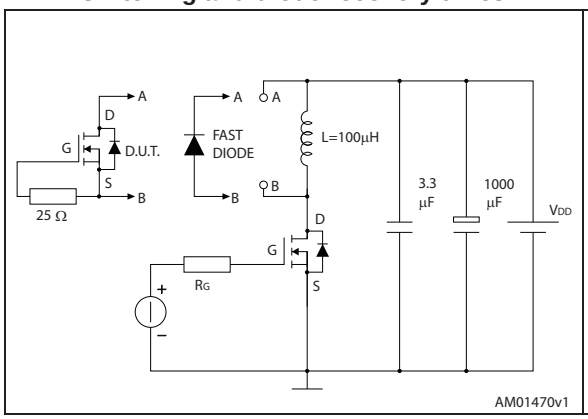


Figure 16. Unclamped inductive load test circuit

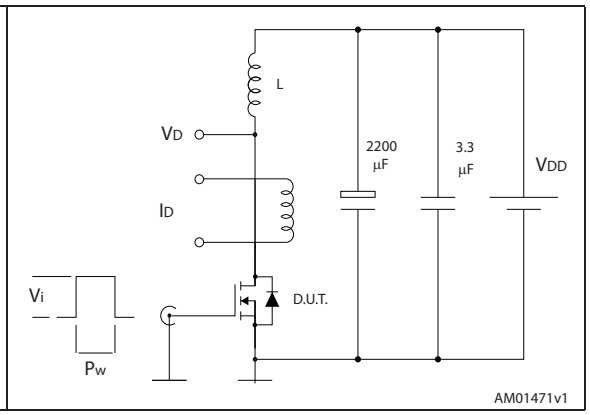


Figure 17. Unclamped inductive waveform

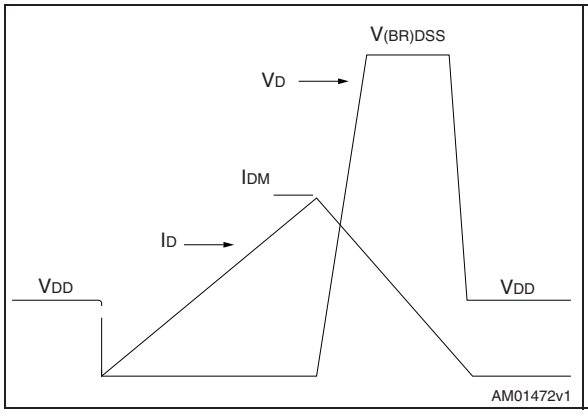
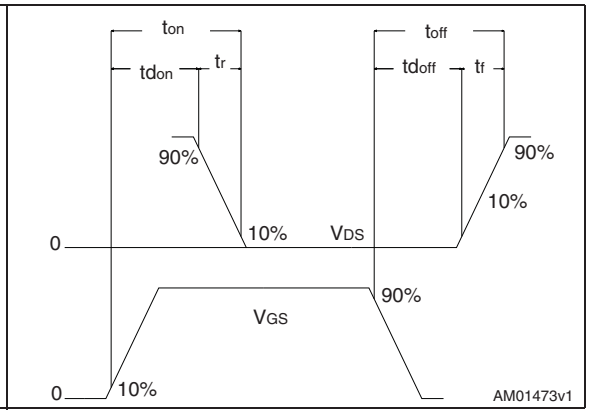


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 19. PowerFLAT™ 5x6 type S-C mechanical data

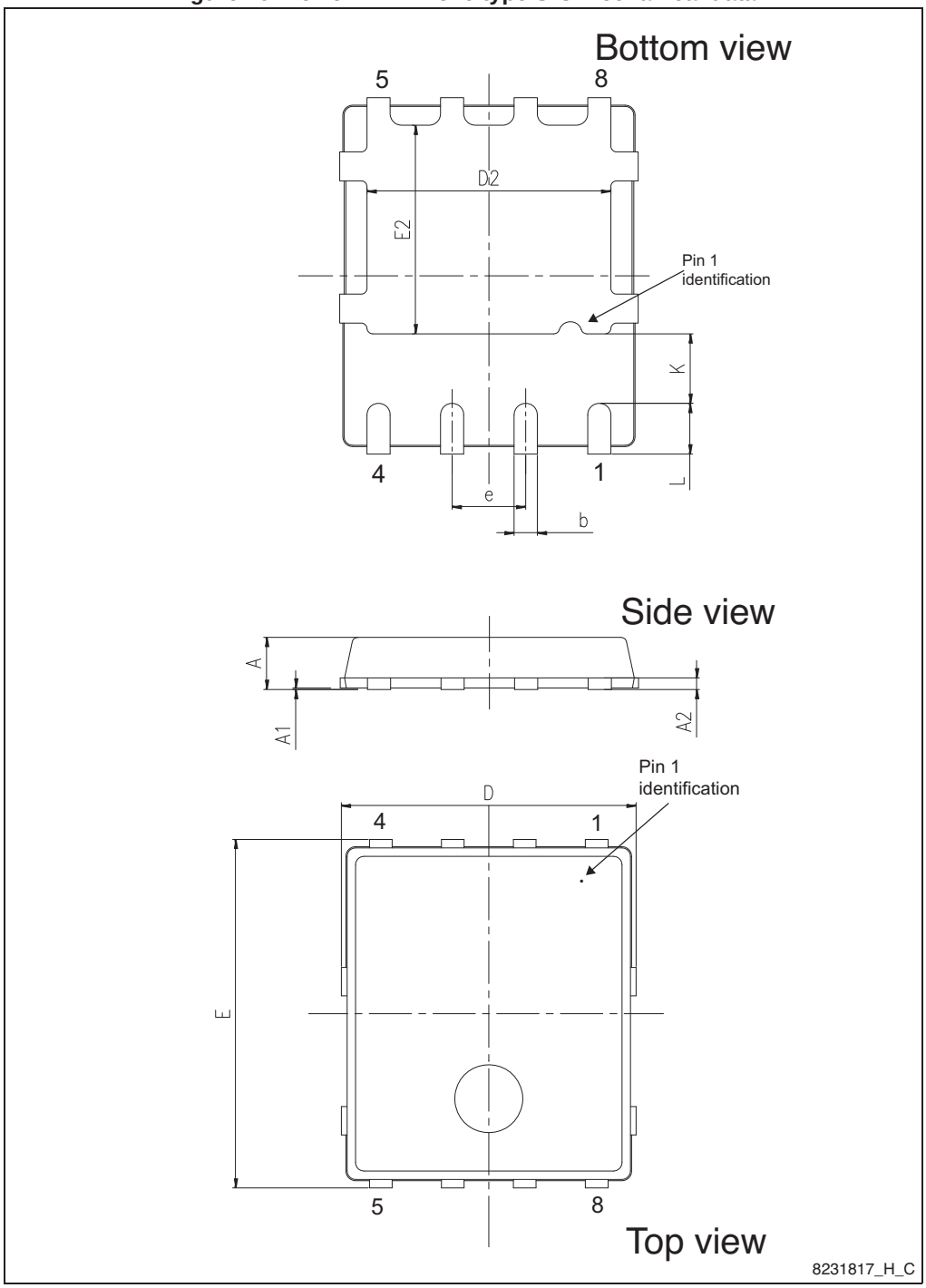
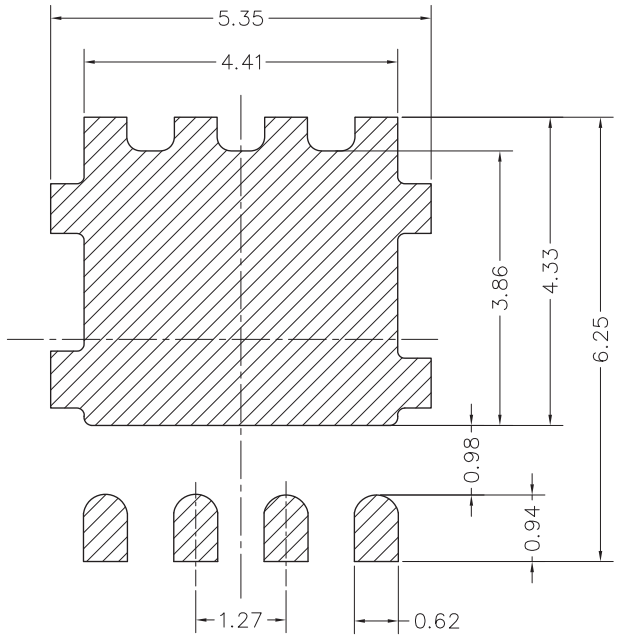


Table 8. PowerFLAT™ 5x6 type S-C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
E		6.15	
D2	4.11		4.31
E2	3.50		3.70
e		1.27	
e1		0.65	
L	0.715		1.015
K	1.05		1.35

Figure 20. PowerFLAT™ 5x6 recommended footprint (dimensions in mm)



Footprint

5 Packaging mechanical data

Figure 21. PowerFLAT™ 5x6 tape[(a)]

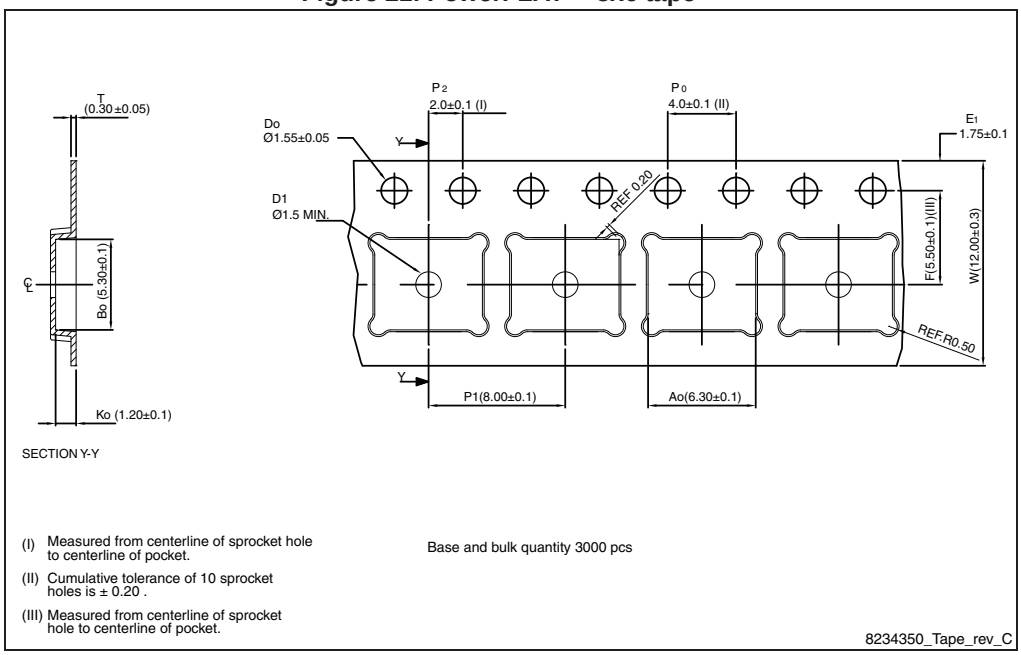
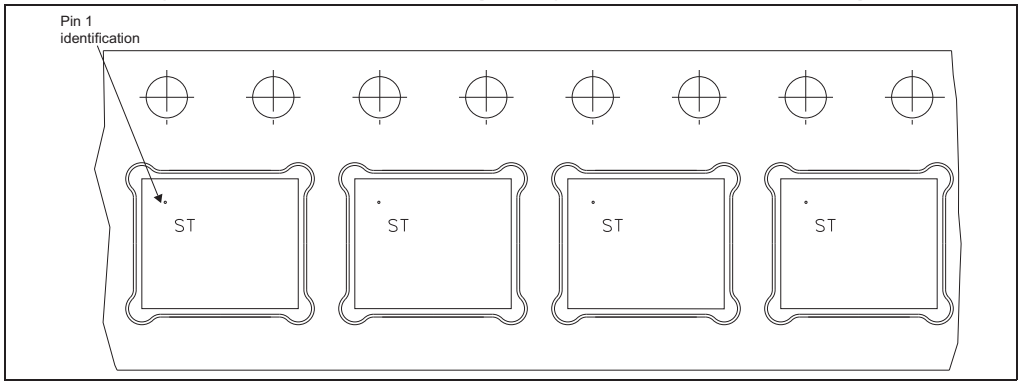
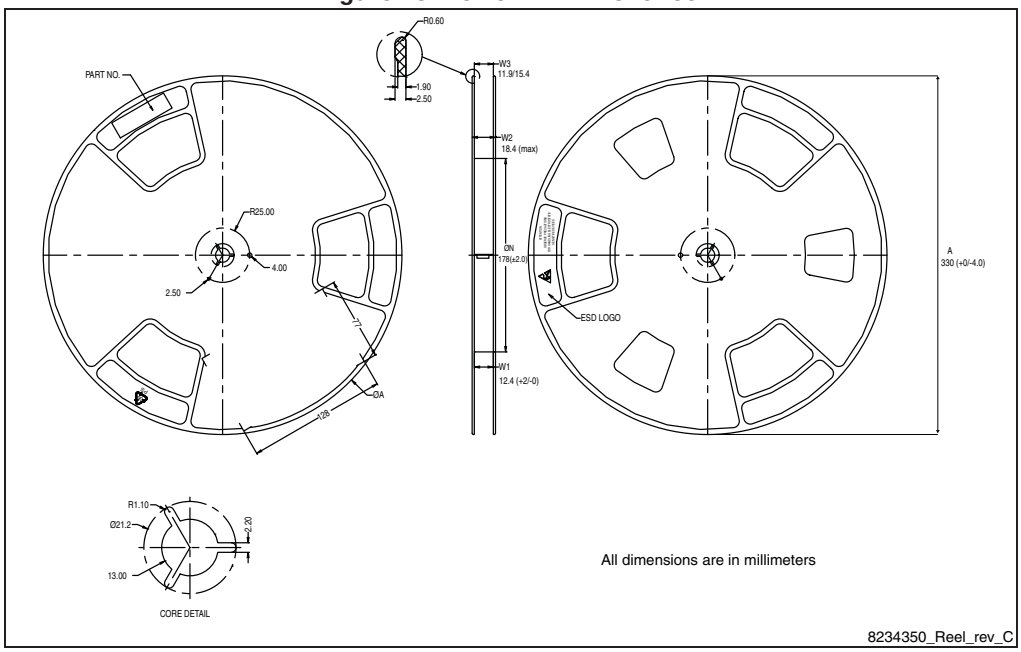


Figure 22. PowerFLAT™ 5x6 package orientation in carrier tape



a. All dimensions are in millimeters.

Figure 23. PowerFLAT™ 5x6 reel



6 Revision history

Table 9. Document revision history

Date	Revision	Changes
04-Jun-2013	1	First release.
11-Jun-2013	2	– Changed: *Description* – Minor text changes
08-Nov-2013	3	– Modified: title, I_D (Drain current (continuous) at T_{pcb} = 100 °C), P_{TOT} (Total dissipation at T_C and T_{pcb} = 25 °C) and T_J values in *Table 2*, $R_{thj-case}$ value in *Table 3*, $V_{(BR)DSS}$ and $V_{GS(th)}$ test conditions, $R_{DS(on)}$ typical values, the entire typical values in *Table 5*, *6*, R_G value in *Table 6*, V_{dd} and typical values in *Table 7* – Updated: *Section 4: Package mechanical data* and *Section 5: Packaging mechanical data*
08-May-2014	4	– Inserted: R_g parameter in *Table 5* – Minor text changes

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